

1

2

3

4

adc
ADC.SchDocfpga
fpga.SchDocMCU
mcu.SchDocAudio
audio-codec.SchDoc

ADC_SHDN
ADC_RAND
ADC_PGA
ADC_DITH

ADC_OFA
REF_CLK_P
REF_CLK_N
ADC_D[0..15]

ATT[0..5]

ADC_SHDN
ADC_RAND
ADC_PGA
ADC_DITH

ADC_OFA
REF_CLK_P
REF_CLK_N
ADC_D[0..15]

ATT[0..5]

nSTATUS
nCONFIG
CONF_DONE
FSPL_nCE
FSPL_DCLK

FPGA_OFA_INT
AUDIO_CLK

FSPL_CS
FSPL_SCK
FSPL_MISO
FSPL_MOSI

FI2S0_WS
FI2S0_CK
FI2S0_SDI
FI2S0_SDO

FI2S1_WS
FI2S1_CK
FI2S1_SDI
FI2S1_SDO

nSTATUS
nCONFIG
CONF_DONE
FSPL_nCE
FSPL_DCLK

FPGA_OFA_INT
AUDIO_CLK

FSPL_CS
FSPL_SCK
FSPL_MISO
FSPL_MOSI

FI2S0_WS
FI2S0_CK
FI2S0_SDI
FI2S0_SDO

FI2S1_WS
FI2S1_CK
FI2S1_SDI
FI2S1_SDO

RESET
PTT0
PTT1
CODEC

PWR_CONTROL
PWR_INT

QSPL_CS
QSPL_CLK
QSPL_IO[0..3]

SD_ENA
SD_INT
SD_CLK
SD_CMD
SD_D[0..3]

WIFI_EN
WIFI_INT
WIFI_TX
WIFI_RX

WIFI_CS
WIFI_SCK
WIFI_MISO
WIFI_MOSI

SDRAM

EXT0_I2C_SCL
EXT0_I2C_SDA

RESET

RESET
PTT0
PTT1
CODEC

power-control
power-control.SchDoc
PWR_CONTROL
PWR_INT

memory
memory.SchDoc
QSPL_CS
QSPL_CLK
QSPL_IO[0..3]

SD_ENA
SD_INT
SD_CLK
SD_CMD
SD_D[0..3]

wifi

wifi.SchDoc

WIFI_EN
WIFI_INT
WIFI_TX
WIFI_RX

WIFI_CS
WIFI_SCK
WIFI_MISO
WIFI_MOSI

sdr

sdr.SchDoc

SDRAM

internal-connectors
internal-connectors.SchDoc
EXT0_I2C_SCL
EXT0_I2C_SDA

EXT1_I2C_SCL
EXT1_I2C_SDA

dac
DAC.SchDoc

DAC_SLEEP
DAC_CLK
DAC_D[0..13]

DAC_SLEEP
DAC_CLK
DAC_D[0..13]

lcd

lcd-rgb.SchDoc

RESET
TP_INT

EXT2_I2C_SCL
EXT2_I2C_SDA
LCD

analog

analog-inputs.SchDoc

AINPUT[0..7]

USB

usb-connectivity.SchDoc

USB_D_N
USB_D_P

USBH_D_N
USBH_D_P

input-devices
inputs.SchDoc

ENC_A
ENC_B

KEY_INT
BTTN0
BTTN1

EXT2_I2C_SCL
EXT2_I2C_SDA

EXT1_I2C_SCL
EXT1_I2C_SDA

ENC_A
ENC_B

KEY_INT
BTTN0
BTTN1

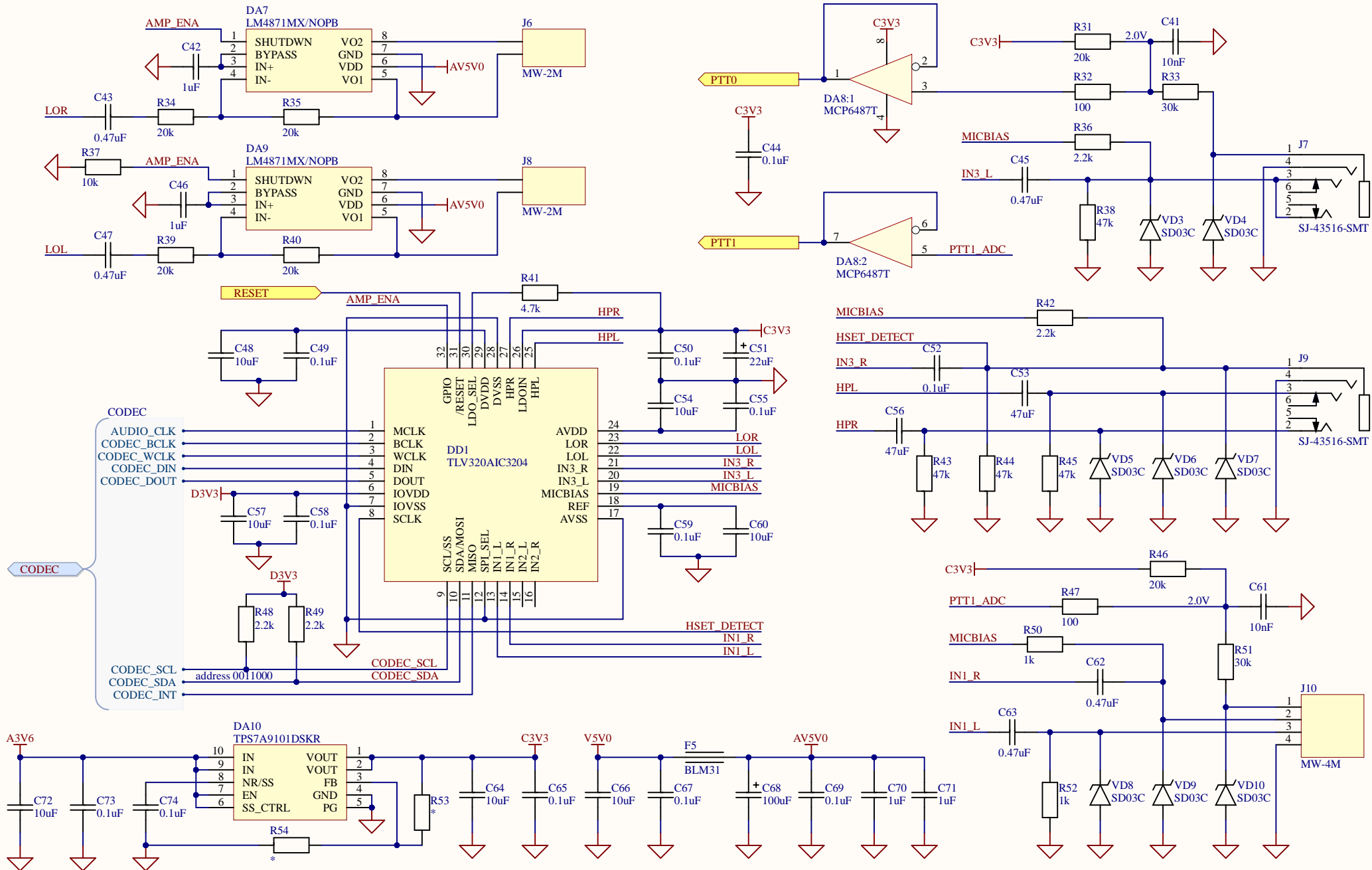
EXT1_I2C_SCL
EXT1_I2C_SDA

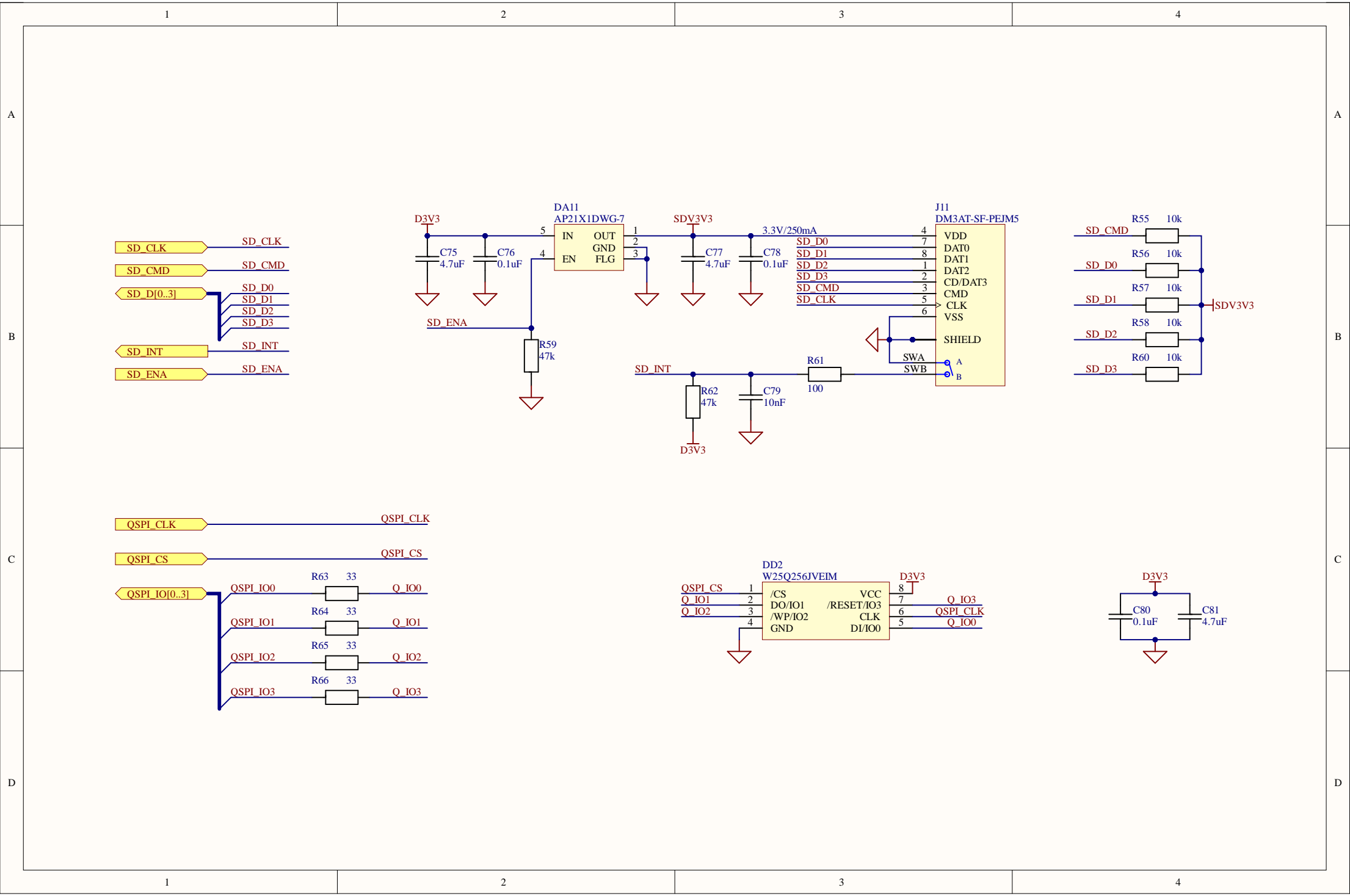
1

2

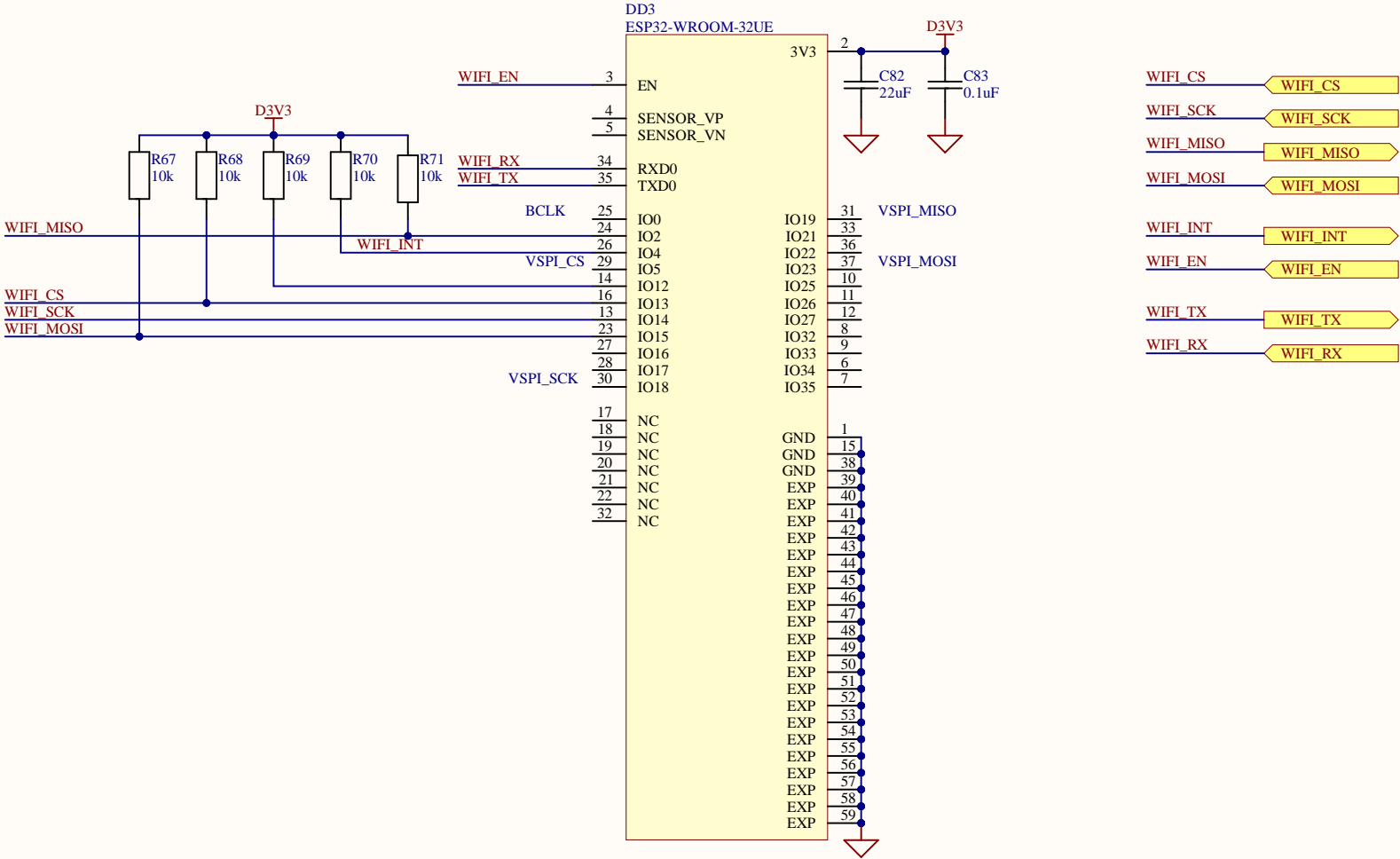
3

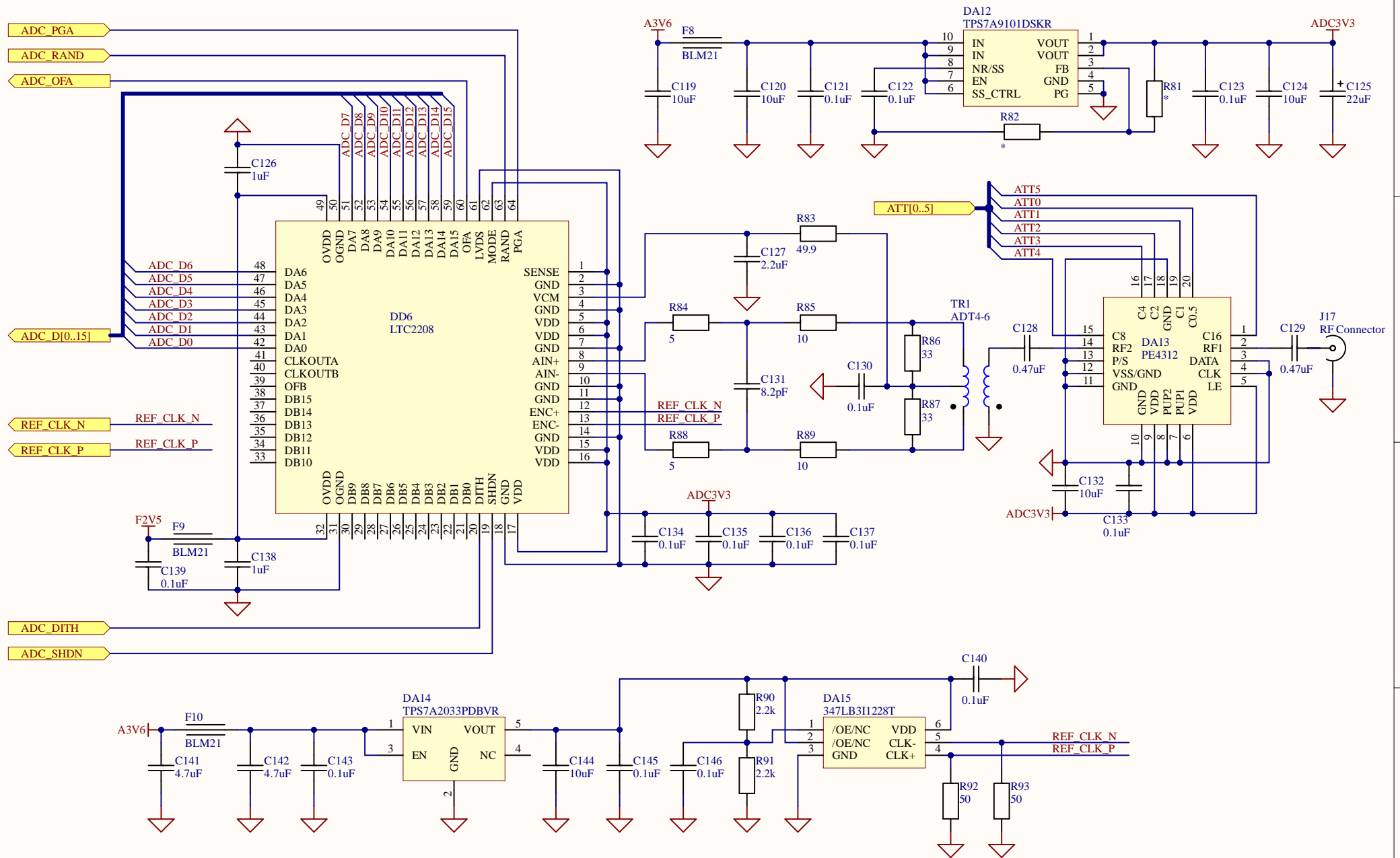
4

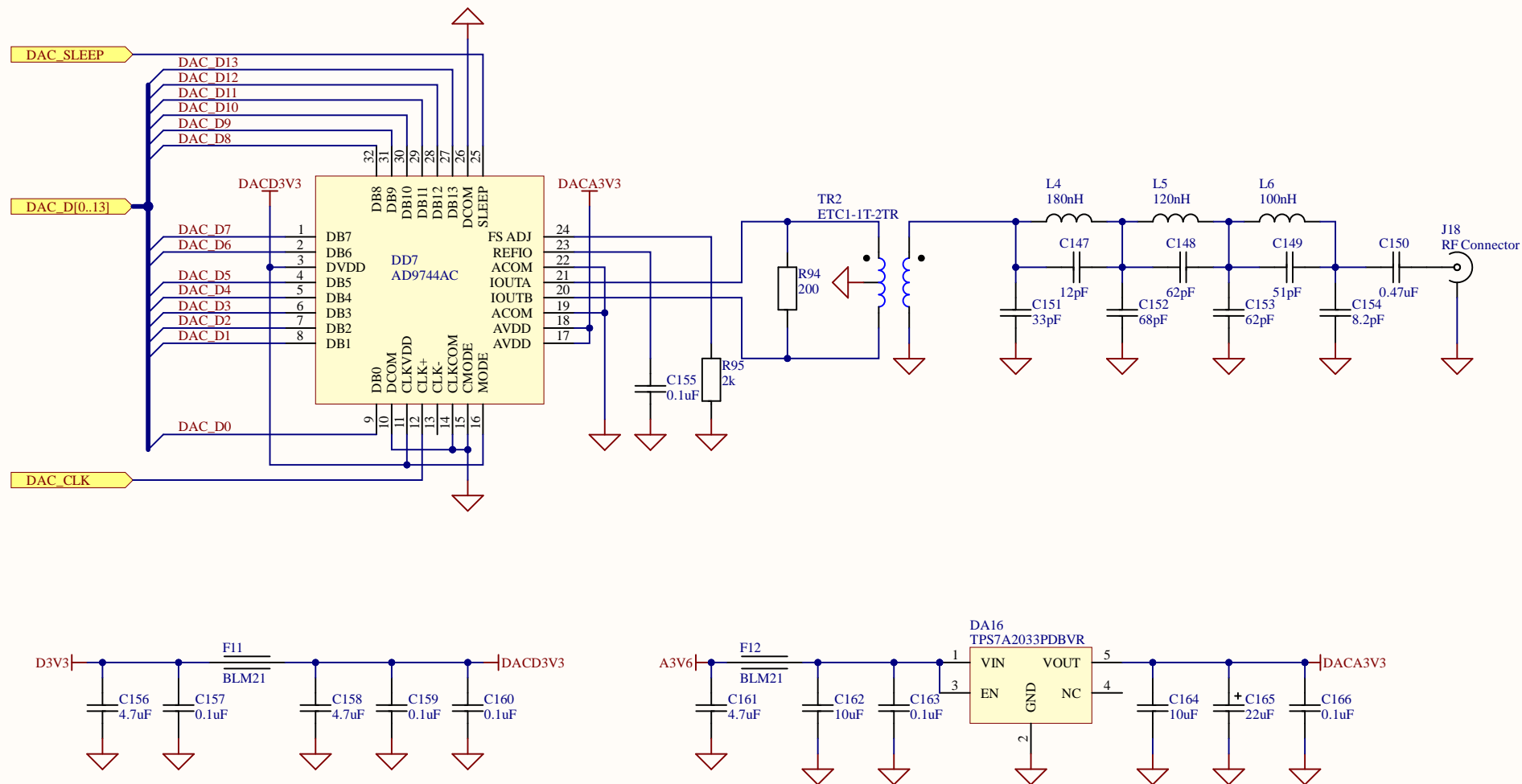


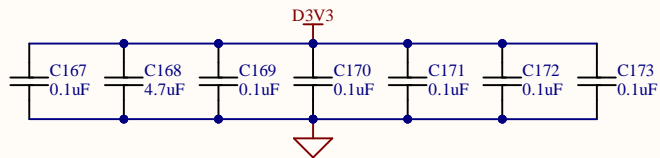
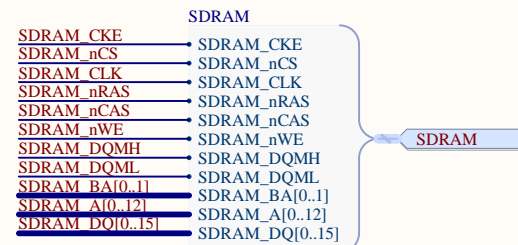
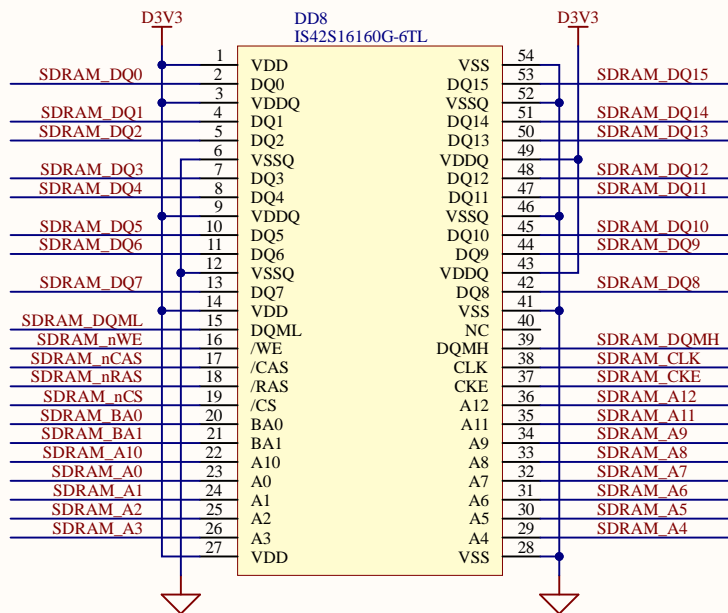


https://docs.espressif.com/projects/esp-idf/en/latest/esp32/api-reference/peripherals/sd_pullup_requirements.html
https://docs.espressif.com/projects/esp-idf/en/latest/esp32/api-reference/peripherals/sdio_slave.html









J19
ER-CON40HT-1

LEDK
LEDA

LCD_R0
LCD_R1
LCD_R2
LCD_R3
LCD_R4
LCD_R5
LCD_R6
LCD_R7
LCD_G0
LCD_G1
LCD_G2
LCD_G3
LCD_G4
LCD_G5
LCD_G6
LCD_G7
LCD_B0
LCD_B1
LCD_B2
LCD_B3
LCD_B4
LCD_B5
LCD_B6
LCD_B7

ER-TFT050-6
ER-TFT070IPS-4

J20
ER-CON10HT-1

D3V3

EXT0_I2C_SDA
EXT0_I2C_SCL
RESET
TP_INT

EXT2_I2C_SDA
EXT2_I2C_SCL
RESET
TP_INT

LCD
LCD_DISP
LCD_DET
LCD_HSYNC
LCD_VSYNC
LCD_R[3..7]
LCD_G[2..7]
LCD_B[3..7]
LCD_DCLK
LCD_BLIGHT

LCD

D3V3

R98
2.2k

R99
2.2k

EXT0_I2C_SCL
EXT0_I2C_SDA

RESET
TP_INT

J21
ER-CON6HT-1

V12V

DAI7

IN
GND
OUT
TAB

2

4

9V

LD1117

R101

100

R103

620

C187

10uF

C188

0.1uF

LCD_BLIGHT

R104

100k

VT3
IRLML9301TRP

LEDA

VT4

NX7002AK

VD11
MBR0540T1

12V-38V

L7

V12V

LCD_BLIGHT

DAI8

VIN

CTRL

SW

FB

COMP

GND

TPS61165

LEDK

C184

0.22uF

R102

*

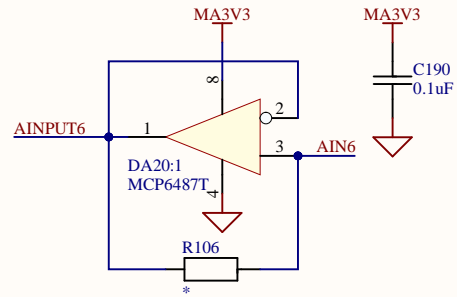
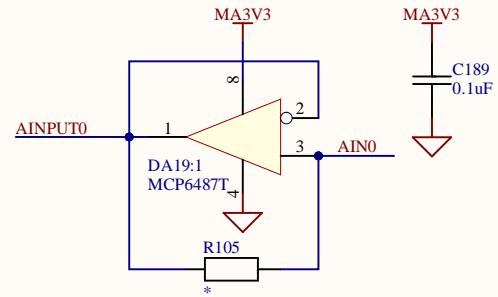
Install if more then 12V is required

1

2

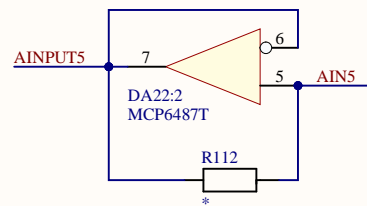
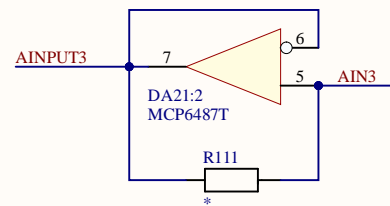
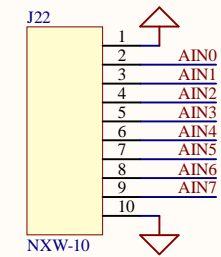
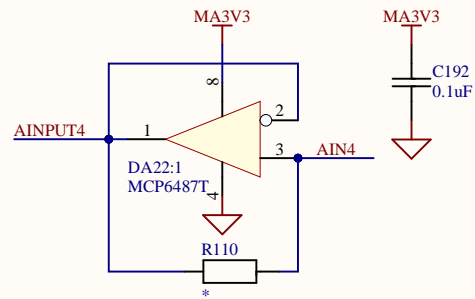
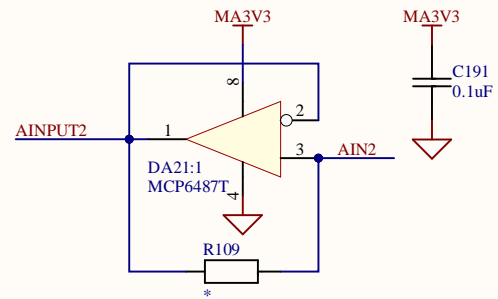
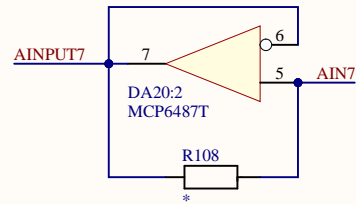
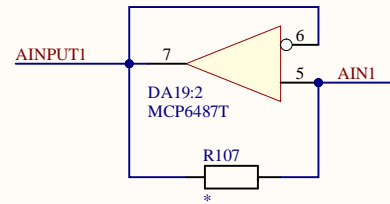
3

4



AINPUT[0..7]

AINPUT[0..7]

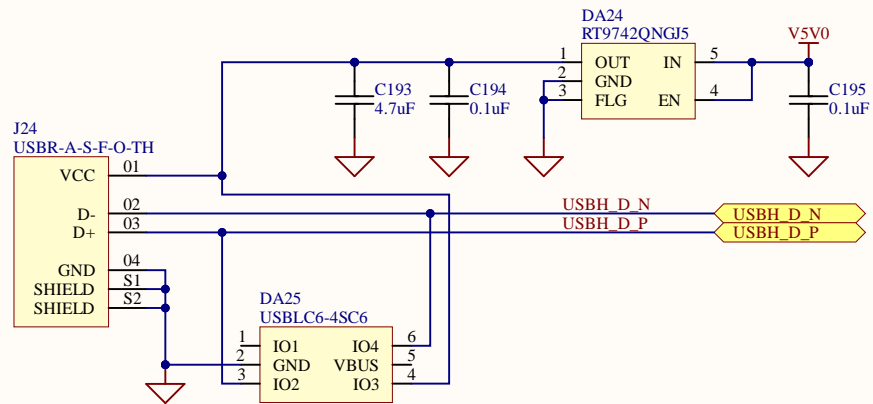
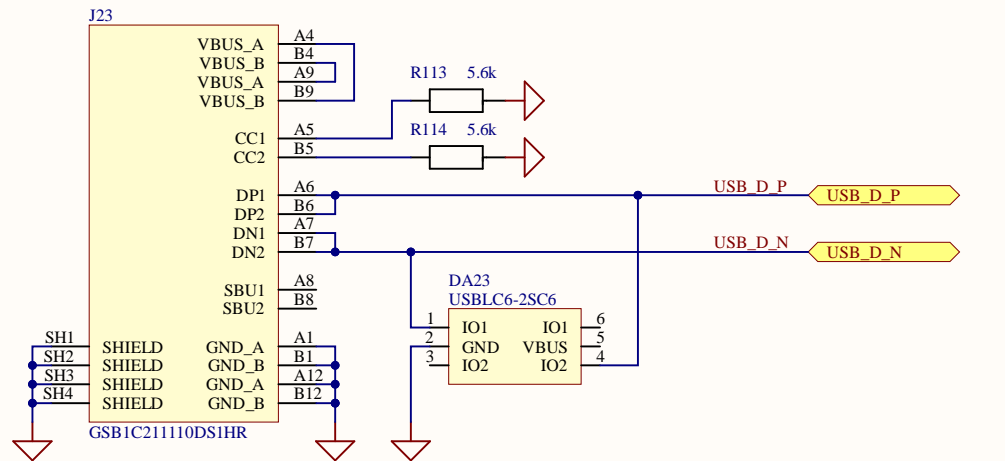


1

2

3

4



1

2

3

4

A

A

B

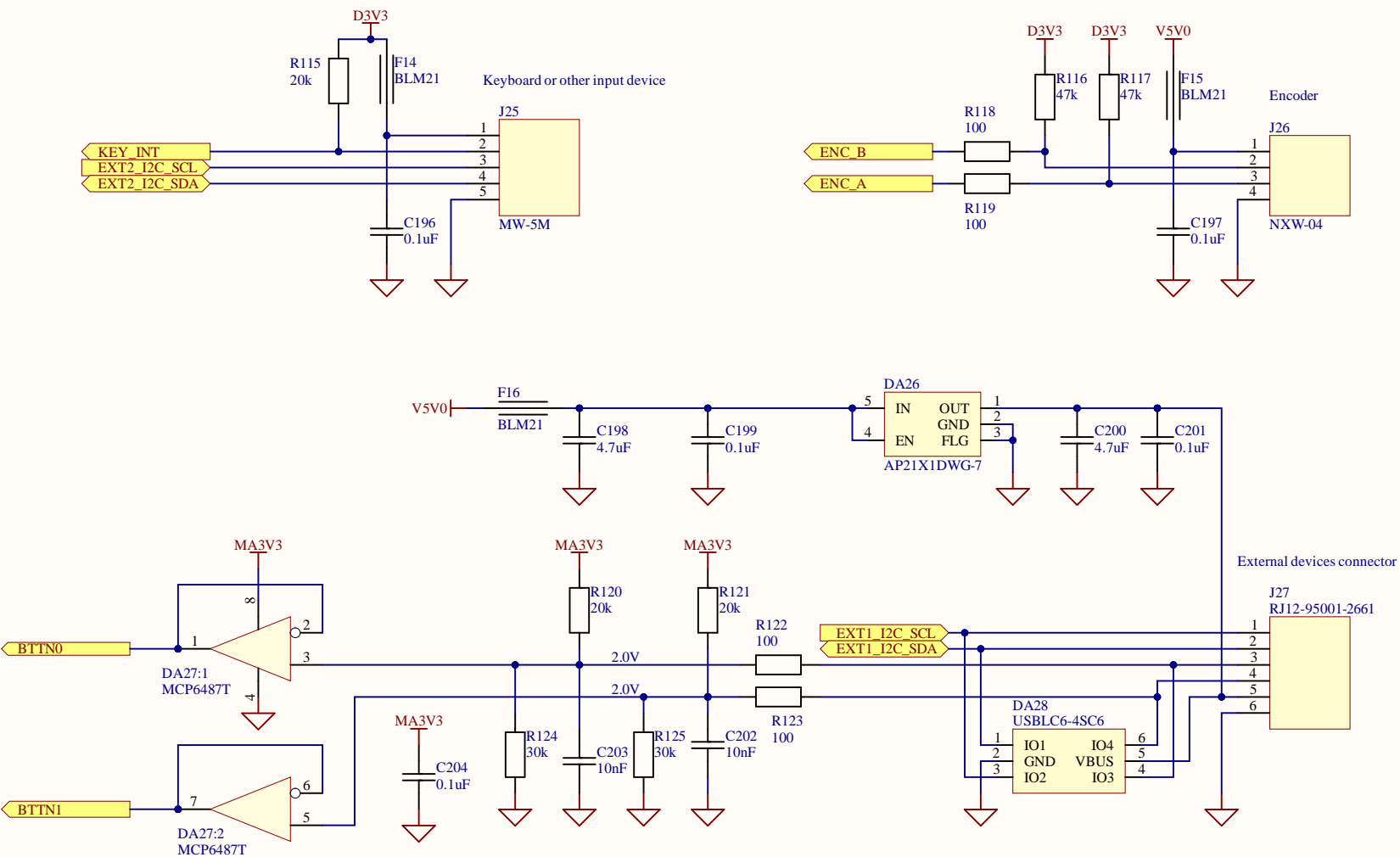
B

C

C

D

D



1

2

3

4

A

A

B

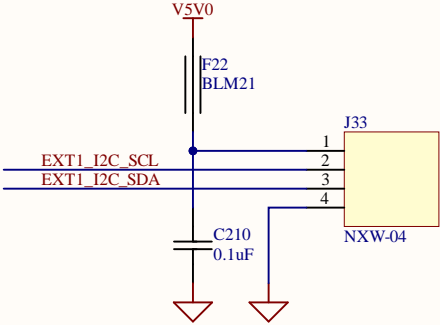
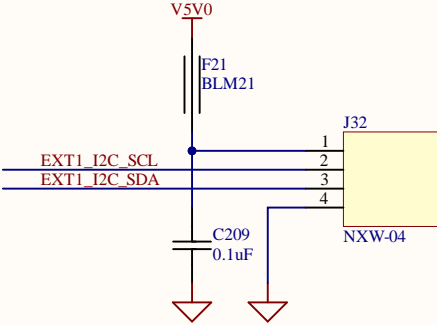
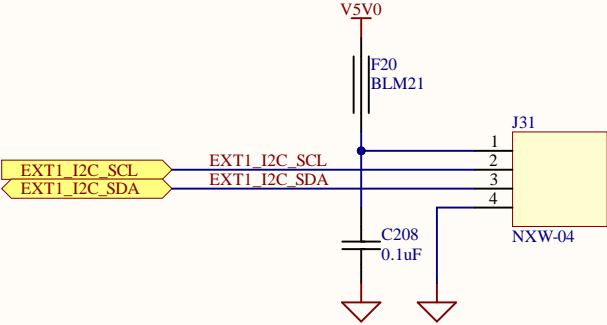
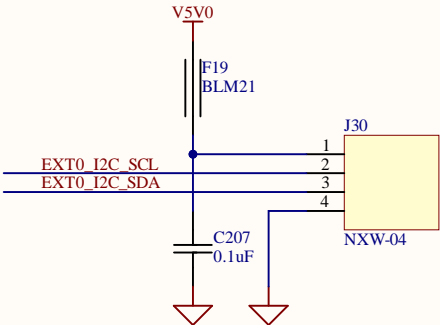
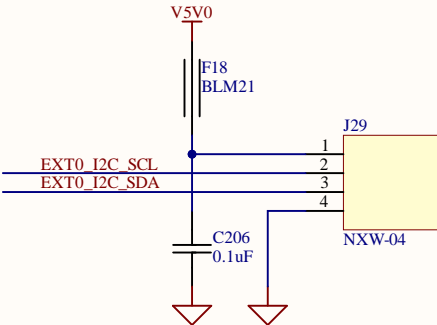
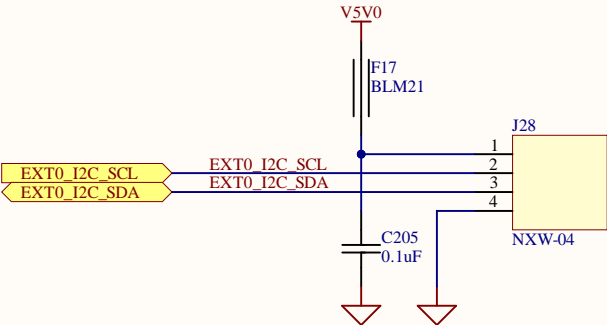
B

C

C

D

D



1

2

3

4

